Phase noise evaluation of DAC for synthesizer applications.

J. Hellén, M. Oskarsson
SAAB Microwave Systems
412 89 Göteborg
Sweden

***Abstract*—Modern commercial D/A-converters are capable of sampling frequencies up to 4000 MHz. This work has been performed to evaluate the spectral purity of a high speed DAC. The aim of the investigation is to verify if a synthesizer built up using a DAC, can match the performance of an analog PLL circuit. The following parameters have been verified: Phase noise, AM-noise and spuriouses.** *(Abstract)*

I. INTRODUCTION

In many applications there is a requirement for both high spectral purity as well as fast frequency switching time. A PLL circuit is often a compromise between high spectral purity and fast frequency switching time. The performance of digital circuits such as DAC and DDS has been improved a lot recently regarding spectral purity and maximum clock frequency. DDS circuits have always been the preferred choice when it comes to frequency switching time. The great disadvantage with these circuits has traditionally been poor spectral purity. Modern circuits however has a good spectral purity, at least according to data sheets. This work has been performed in order to find out if a digital synthesizer can match the performance of an analog PLL.

II. CIRCUIT TOPOLOGY

The required output frequency from the synthesizer shall be 800 MHz with a frequency tuning bandwidth of TBD MHz. There are no commercial available DDS circuits capable of such high output frequencies, however high speed DAC:s exists from several manufactures. A digital synthesizer can be built using a FPGA circuit to feed the data to a high speed DAC.

III. CLOCK FREQUENCY

It is essential for the spectral purity of the output signal to select an appropriate clock frequency for the DAC. The optimum clock frequency will be different for different output frequencies. To achieve good spectral purity performance the following harmonics / sub harmonics of the clock and the output frequencies should be avoided inside the desired frequency band:

Fclk / 2 (1)

Fclk / 4 (2)

Fclk/2 – Fout (3)

Fclk -2Fout (4)

Fclk – 3Fout (5)

Fout + clk/4 (6)

To fulfill the conditions above we have to use a high clock frequency close to 4000 MHz when generating a frequency band centered around 800 MHz. We decided to use 4000 MHz since it fulfills the above conditions but also to verify the performance of the DAC at its maximum specified clock frequency.

IV. EVALUATION BOARD

An evaluation board has been designed to be able to generate the LVDS input signal to the DAC. An alternative solution could have been to use a high speed pattern generator to generate the LVDS signal. A disadvantage with a pattern generator is that we will not be able verify the DAC under realistic conditions that is conditions as it will be used in a possible future product.

The evaluation board in figure 1 below consists basically of a FPGA circuit with an external boot memory and the DAC. On the board there are also some power supply circuits.

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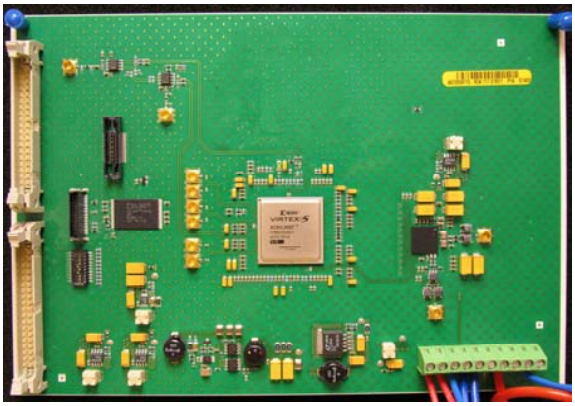

Figure 1. Picture of evaluation board.

In figure 2 below a basic block diagram of the board is presented. The input clock (CLK) of the board is connected to the DAC. Out from the DAC there is also a frequency divided clock of 500 MHz that runs the FPGA. Internally the FPGA runs on a 100 or 500 MHz clock. All clock signals on the board are synchronized. The frequency control word (FREQUENCY) is connected to the NCO (Numerical Controlled Oscillator) logic that works basically as an address generator. The output addresses from the NCO logic controls the phase increment, for the selected frequency. This is performed by addressing the register in the ROM logic were the appropriate phase value is stored. The DDR logic works mainly as a 40:4 MUX were the 40x12bit address bus running at 100 MHz gets transformed to 4x12bit address bus running at 500 MHz or 1 GBit/s since they are double data rate. Internally in the DAC there is a 4:1 MUX. The reason for using the MUX technique is to reduce the data speed to levels that the FPGA can handle internally.

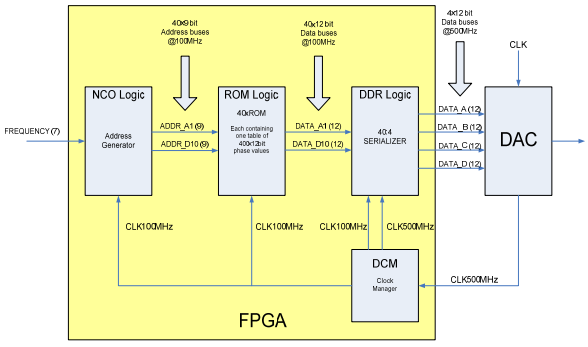

Figure 2. Block diagram of evaluation board.

V. SPUR EVALUATION

Besides the harmonic spurs described in chapter 3 there will also be spurs from the synthesis fractionallity. Using a clock frequency of 4000 MHz, as described in chapter 3, and for example a channel spacing of 10 MHz gives that the phase table stored in the ROM need to have 400 phase values. If all 400 phase values are sampled using a clock frequency of 4000MHz we will have an output frequency of 10 MHz and if we use every second phase value in the table, still using the same clock frequency, we will of course have an output frequency of 20 MHz. To generate an output signal of 800 MHz every 80th phase value in the phase table will be used. The spurs from the fractionallity will be different for each selected output frequency. In table 1 below the spurs from the fractionallity for a number of output frequencies are presented.

Table 1. List of spur

Output Frequency (MHz)	Fractionallity	Spur (Frequency fromCarrier) (MHz)
750	75/400 = 3/16	250
760	76/400 = 19/100	40
770	77/400	10
780	78/400 = 39/200	20
790	79/400	10
800	80/400 = 1/5	800
810	81/400	10
820	82/400 = 41/200	20
830	83/400	10
840	84/400 = 21/100	40
850	85/400 = 17/80	50

In the following plots, figure 3-5, we can se the measurement results of spurs for some frequencies. The spur at 1000 MHz is the Clk / 4.

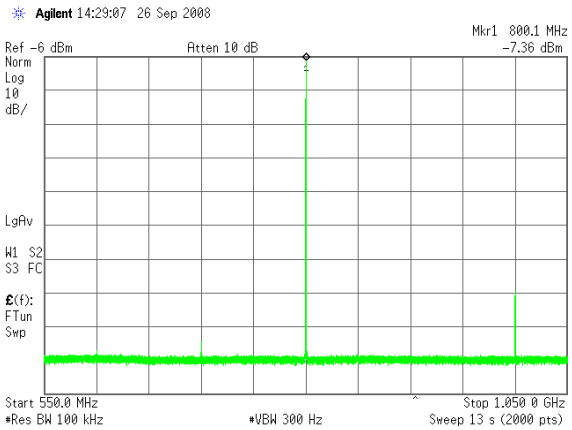

Figure 3. Spur plot for 800 MHz output frequency

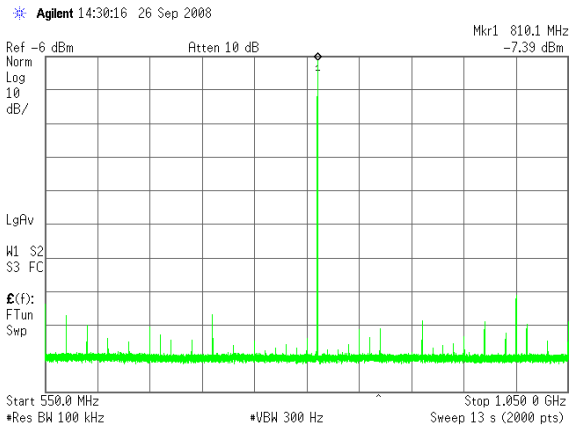

Figure 4. Spur plot for 810 MHz output frequency

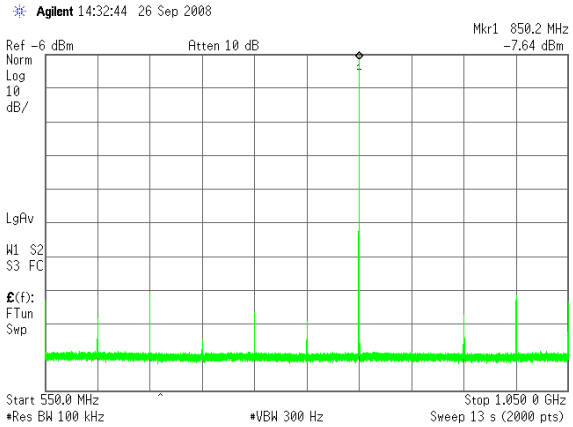

Figure 5. Spur plot for 850 MHz output frequency

VI. PHASE NOISE EVALUATION

The residual phase noise of two evaluation boards has been measured. Since we are measuring the sum of the phase noise from two boards, 3 dB has been subtracted from the results in the following phase noise plots. In figure 6 below the block diagram of the measurement setup is presented. In this measurement the DAC-boards are regarded as a frequency divider where the clock is the input signal and the output signal of for example 800 MHz is measured. Since this is a residual phase noise measurement the phase noise contribution from the clock is cancelled out.

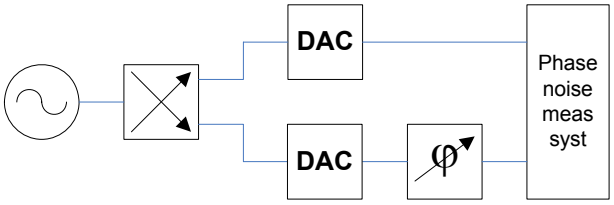

Figure 6. Block diagram of measurement setup

In figure 7 below we can se the residual phase noise plot of the IF signal generated by the DAC. As can be seen the spectral purity is good, except for the power supply noise of n x 50 Hz there are no other spurs present. The phase noise floor is about -152 to -158 dBc / Hz and close to carrier we have a 1/f noise. Around 10 KHz from carrier we can se a slight phase noise degradation that originates from power supply noise.

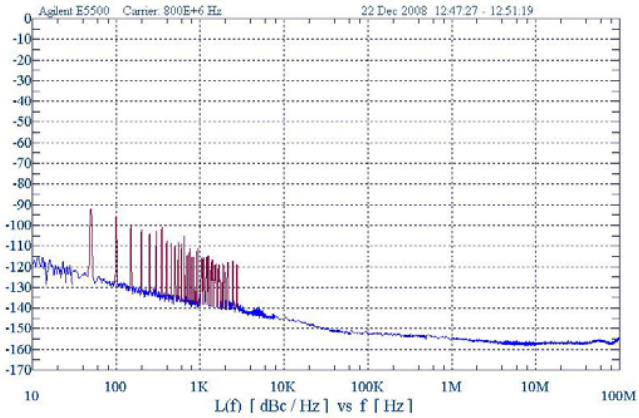

Figure 7. Phase noise @800 MHz Clk 4000 MHz

In figure 8 below the phase noise for an output signal of 810 MHz is presented. The result is rather similar to the previous one except that we now have spurs at nx10 MHz from the fractionallity present.

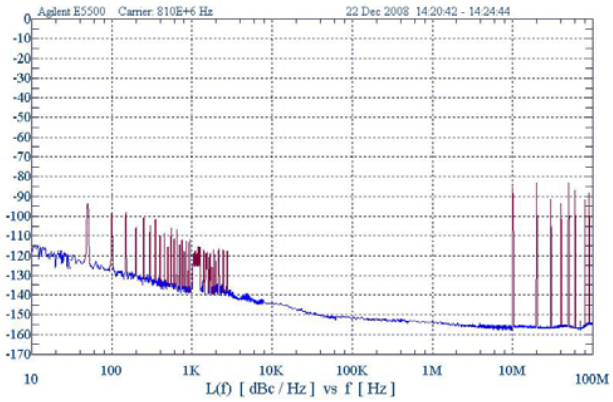

Figure 8. Phase noise @ 810 MHz Clk 4000 MHz

VII. AM NOISE EVALUATION

The AM noise of the output signal have also been measured. In figure 9 below the result for an output signal of 800 MHz is presented.

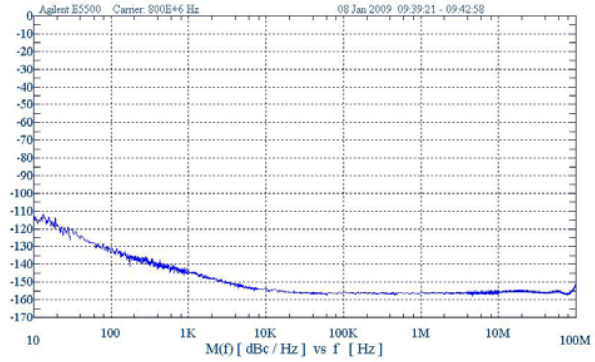

Figure 9. AM noise @ 800 MHz Clk 4000 MHz

VIII. CONCLUSION

An evaluation board containing a digital synthesizer has been designed and evaluated. The overall result of the evaluation looks very promising. In figure 10 the residual phase noise of the DAC is compared with typical noise levels of a frequency multiplied 100 MHz SC-cut crystal oscillator. As can be seen in the graph the results are rather similar except for offset frequencies of 10 KHz were the performance of the digital synthesizer is somewhat worse. Also the spur performance is similar to what can be expected from an analog synthesizer. Overall the performance measured on this evaluation board show that a digital synthesizer can be an alternative to an analog one. A great advantage with the digital synthesizer is of coarse its superior frequency switching time. However the implementation has not been easy. We have had major problems with timing between the data inputs to the DAC, 96 input signals running at 1Gbit/s. Also the timing between FPGA data and the DAC clock has been troublesome.

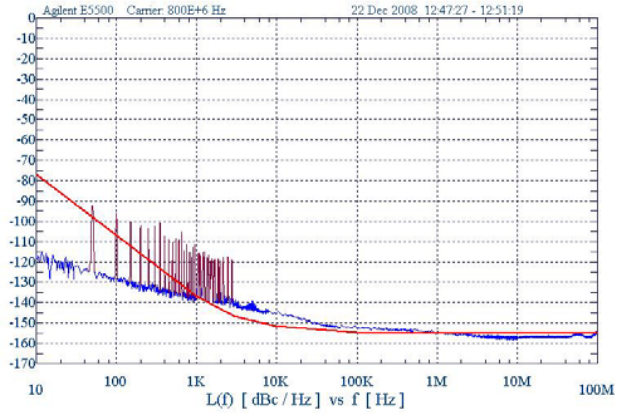

Figure 10. Comparison analog vs. digital synthesizer.

REFERENCES

[1] None